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A 64-Channel ASIC for In-Vitro Simultaneous Recording and Stimulation of Neurons using Microelectrode Arrays

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Abstract— A 64 channels CMOS chip dedicated to in-vitro simultaneous recording and stimulation of neurons using microelectrode arrays has been developed. It includes, for each channel, a low noise, variable gain (10, 75 or 750), 0.08Hz-3kHz bandwidth measurement path with unity-gain for lower frequencies to allow measurement of the electrochemical potential. A snapshot style Sample & Hold circuitry allows to have "images" of the 64 channels at a maximum sampling frequency of 50kHz. Input-referred noise of the measurement path is 4.3µV RMS integrated from 0.08Hz to 3kHz. To get rid of the random, slowly varying, DC offset potential that exists at the electrode-electrolyte interface, the ASIC can be supplied with floating VSS, VDD. Circuit size is 2.4mm per 11.2mm (0.35µm CMOS process) and its power consumption is about 125mW.

I. Introduction

Deciphering the neural code remains a major challenge of nowadays Neuroscience. As information within the Central Nervous System is distributed over large populations of neurons, recording the activity of multiple cells simultaneously is mandatory to understand the dynamics of large neural networks [1], [2]. Microelectrode arrays (MEAs) provide an elegant way to probe electrical activity over large populations of neurons either *in vitro* or *in vivo* and also offer the possibility to deliver electrical stimulation to neural networks, which may become a key treatment of several neurological diseases symptoms. Interfacing neurons through MEAs using discrete electronics rapidly limits the number of channels, especially in small animals like mice, bringing up the need for highly integrated electronics to reach sufficient spatial resolution. Compared to current state of the art [3], [5], we developed an ASIC allowing simultaneous recording and stimulation for up to 64 channels with eight different stimulation patterns and measurement of both electrochemical potential and neural activity with limited artifacts sensitivity using a blanking technique.

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II. ASIC Architecture

Fig. 1 shows one channel architecture of the manufactured 64-channel ASIC. Each channel includes a low noise, variable gain measurement path, Sample & Hold circuitry, 6-bit configuration register, an 8 to 1 multiplexer and a voltage to current converter for stimulation feature.

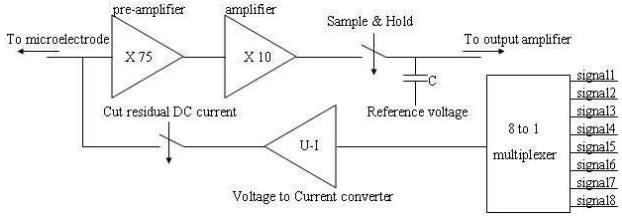

Fig. 1 : Architecture of one channel

A. Measurement Path

As shown on Fig. 2, preamplifier and amplifier are based on the same structure providing unity DC gain and AC gain of respectively 75 and 10 in a theoretical 1Hz to 3kHz bandwidth; both can be separately switched to follower configuration to have four different gains (1, 10, 75, 750), allowing a good sensitivity measurement of biological signals from different points of the microelectrode array. Each channel includes two dedicated autonomous current biasing for preamplifier and amplifier.

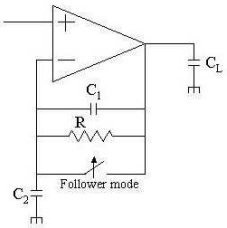

Fig. 2 : Amplifier architecture

Unlike the common approach of high-pass filtering the electrochemical potential [3], [4], [5], this ASIC allows the measurement of the slowly varying input DC voltage, what might become very useful to gather informations about the interface stability and quality (electrochemical, mechanical and biological point of view).

Low cutoff frequency of the preamplifier is achieved using diode-connected PMOS transistors [4], the same structure is used for the amplifier but with five devices in series in order to reduce signal distortion due to a higher voltage swing between input and output.

Measured input-referred noise of one channel through the whole test bench is 4.3µV RMS with a power consumption of 75µW, measured signal bandwidth is about 0.08Hz to 3kHz with good homogeneity between channels.

B. Stimulation Path

Electrical stimulation can be used to dynamically elicit neural activity. A pattern-tolerant architecture which can deliver a biphasic current independently of the neuron's impedance is preferred. In this ASIC, stimulation is achieved by using, in each channel, an 8 to 1 multiplexer (fed by 8 external voltage input signals for the whole ASIC) and a voltage to current converter allowing uniform current stimulation (+/- 400µA peak maximum). Measured transfer function of voltage to current converters, with V_{SS}=-2.5V and V_{DD}=+2.5V, shows good linearity and limited drift between channels (Fig. 3). A global control signal has been added to cut the residual DC current, after stimulation patterns have been applied, by means of a switch at the output of the 64 voltage to current converters in order to prevent any damaging of the cells. Dedicated power supply can be shut down to reduce power consumption when stimulation functionality is not in use.

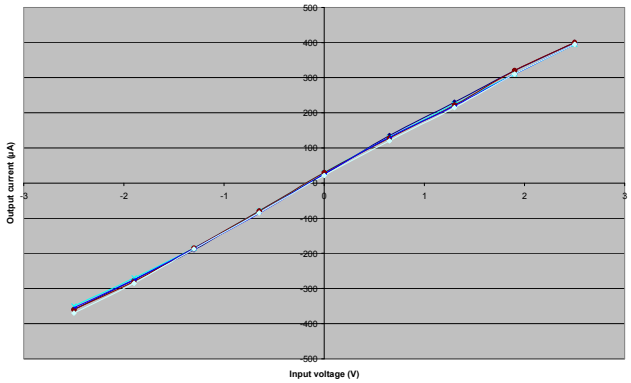

Fig. 3 : Transfer function of the voltage to current converter for several channels

C. Digital Control Circuit

The ASIC is configured using a static serial configuration register with six bits for each channel (two bits to choose the gain, three bits to choose the stimulation signal and one last bit to activate stimulation).

As stimulus artefacts are usually several orders of magnitude larger than neuron's signal, they may saturate the input of the measurement path, with some kind of paralysing effect on the signal recording functionality. In order to reduce this effect, blanking technique can be implemented by setting the desired channel measurement path in follower mode, pre-loading static configuration registers during stimulation and loading the configuration effectively after a preset period of time to apply gain as described in [6]. In this case, there is no amplification of the large input signal variation during stimulation and bandwidth of the amplifiers is wider for faster response (thus shorter paralysed state).

D. Sample & Hold and output amplifier

A snapshot style Sample & Hold circuitry has been implemented to have "real images" of the 64 channels (no delay time between each of them as in sequential reading) at a maximum sampling frequency of 50kHz, which leads to a total data output frequency of 3.2MHz (time-multiplexed on a single output).

Output amplifier is connected as shown on Fig. 4, sampled data being transferred one after the other as a charge packet from the sampling capacitor of each channel to the feedback capacitor of the output amplifier. This structure saves some silicon area and power consumption as it avoids the implementation of one bus driver in each channel.

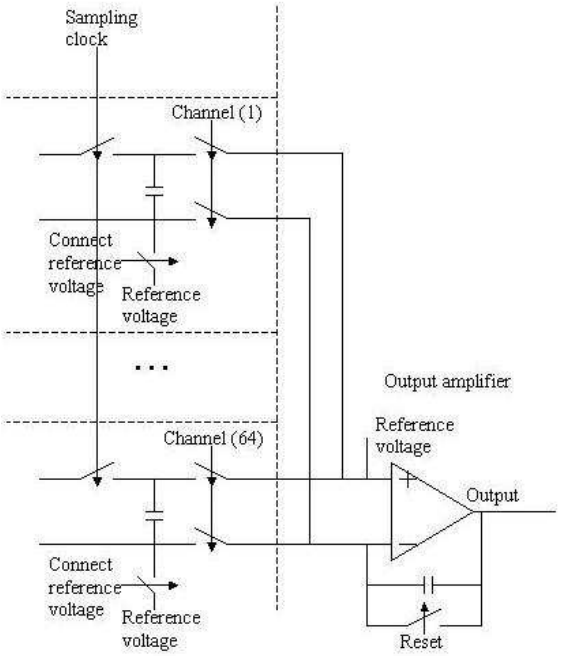

Fig. 4 : Architecture of the output amplifier

III. Biological Measurement Results

A. ASIC integration into the BioMEA™ system

This ASIC is part of the BioMEA™ system which comprises up to four 64-channel ASICs, a high density microelectrode array (256 3D-microelectrodes), specific acquisition boards, and a user-friendly software for data acquisition and visualization as shown on figure 5.

The recording and stimulation electronics controls include ASIC analog output signal level-shifting (as the ASIC can be supplied with floating V_{SS}, V_{DD} to get rid of the electrochemical potential), 14 bits analog to digital converters for data acquisition, 14 bits digital to analog converters for stimulation patterns generation. The system also provides an adjustable power supply for all ASICs.

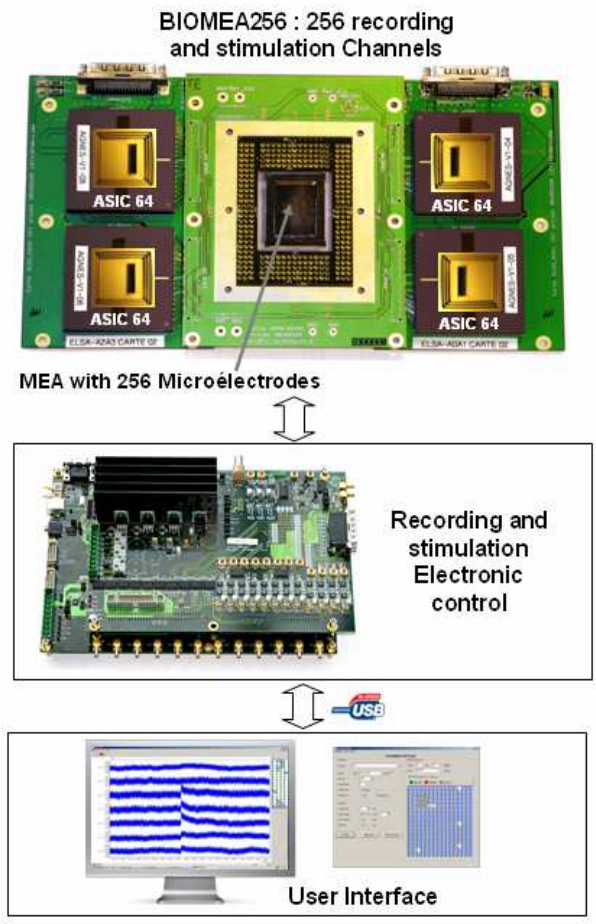

Fig. 5 : BioMEA™ system setup

B. Neural measurements

Developing neural networks generate spontaneous activity that is important for the maturation of a functional circuit. We have been using microelectrode arrays to record from a whole embryonic mouse hindbrain-spinal cord preparations isolated in vitro at embryonic days E13-E16.5.

Spontaneous activity was found in the medulla characterized by local field potentials (LFP) recurring every 1-3 minutes. Fig. 6 shows four channels in the same zone with this biological activity and one channel without. This activity, which resembles sharp waves found in the cortex, could be suppressed by a pharmacological blockade of AMPA/Kainate glutamatergic receptors using CNQX (10µM).

A more detailed spatiotemporal mapping of these spontaneous LFP could be obtained using a 256-electrode array (Fig. 7). Maps were built using surface spline interpolation [7].

IV. Conclusion

We have presented an innovative 64-channel ASIC offering the possibility to record from and to stimulate on 64 micro-electrodes with eight different user-defined current patterns. Transfer function of the amplifiers allows measurement of the electrochemical potential, thus giving informations about the quality and stability of the interface during biological activity recording. A blanking technique has been implemented to reduce the dead-time between stimulation and measurement. Moreover, to deal with this random, slowly-varying, DC offset potential due to the electrode-electrolyte interface, the ASIC can be supplied with floating V_{SS}, V_{DD} (with respect to a single equation : $V_{DD} = V_{SS} + 5V$). The Circuit size is 2.4mm per 11.2mm in 0.35µm 2P/4M HR POLY CMOS process and consumes 125mW with 5V power supply. Table 1 gives a summary of the measured performances of the ASIC.

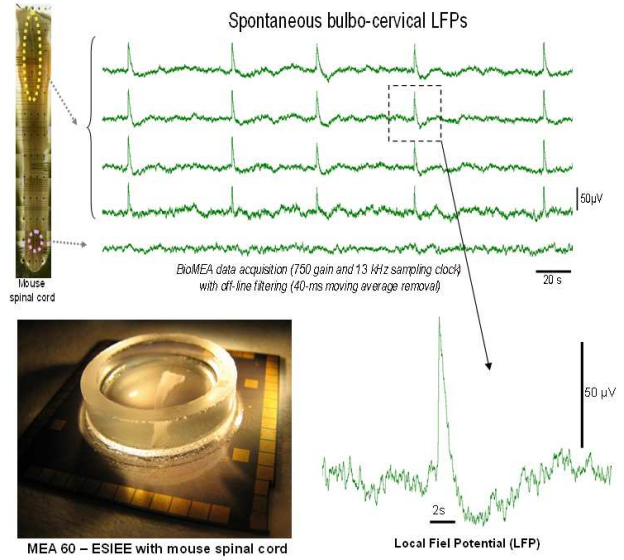

Fig. 6 : Recording of spontaneous bulbo-cervical Local Field Potential (LFP)

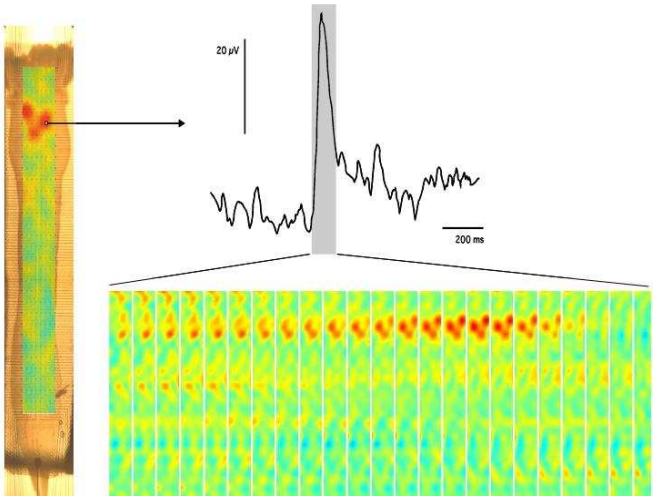

Fig. 7 : Map of mouse spinal cord activities acquired with a 256 microelectrode array and the BioMEA™ system.

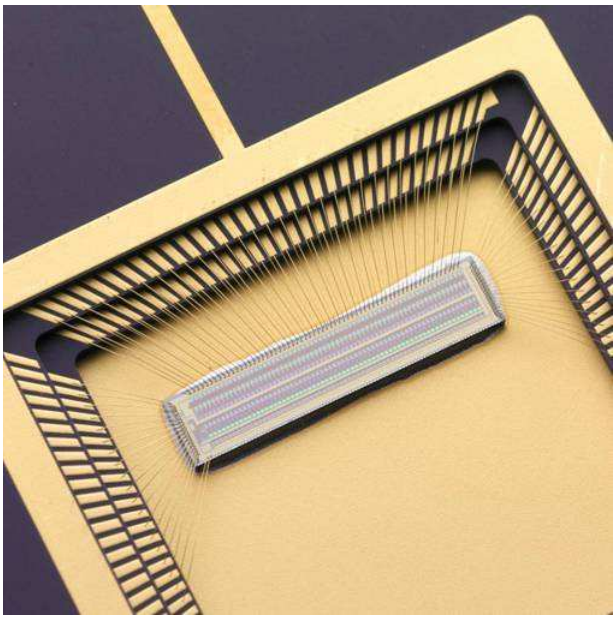

Fig. 8 : Chip photography

TABLE I
SUMMARY OF THE MEASURED PERFORMANCES OF THE ASIC

Parameter	Result
Power consumption	125mW
Input-Referred Noise	4.3µV RMS
Signal Bandwidth	0.08Hz to 3kHz
Maximum Sampling Frequency	50 kHz
Maximum Multiplexing Frequency	3.2 Mhz
Input Impedance	$> 10^{12}$ ohms
Variable Gain	1, 10, 75, 750
Maximum Stimulation Current	+/- 400µA
Area (in 0.35µm CMOS)	27mm²

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